FEATURES

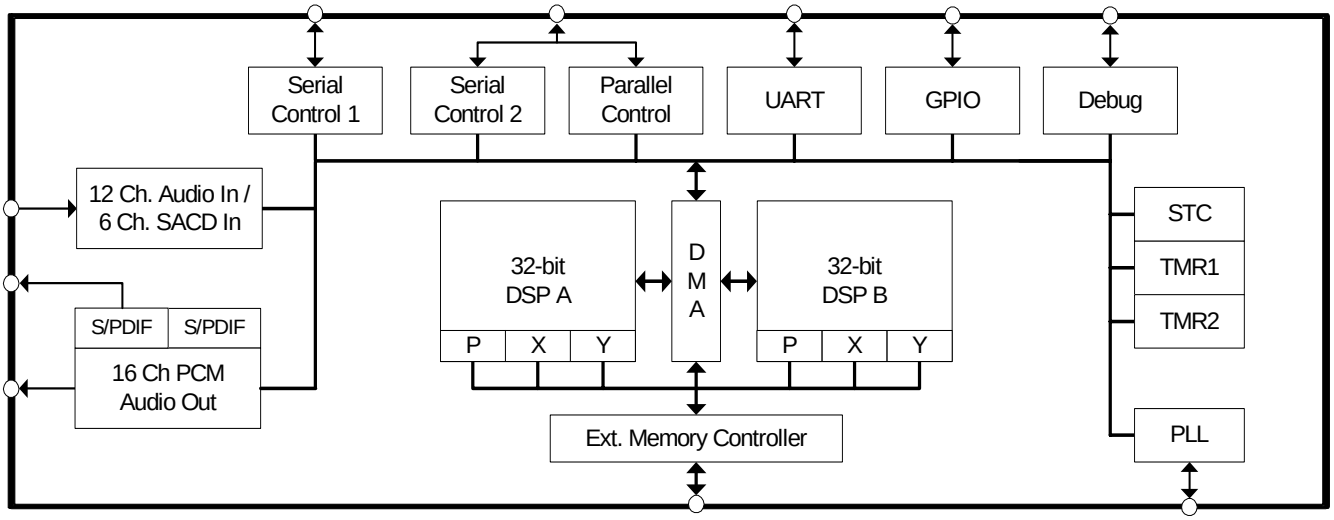
- Multi-standard 32-bit Audio Decoding plus Post Processing
- Framework™ Applications Library in ROM
  - Dolby Digital® EX, Dolby® Pro Logic® IIx, Dolby Headphone®, Dolby® Virtual Speaker®
  - DTS-ES 96/24™, DTS-ES™ Discrete 6.1, DTS-ES™ Matrix 6.1, DTS:Neo6™
  - AAC™ Multichannel 5.1
  - SRS® CS2® and TSXT®
  - THX® Ultra2™, THX® ReEQ™
  - Cirrus Original Multi-Channel Surround (COMS)
  - Crossbar Mixer, Signal Generator
  - Advanced Post-Processor including: 7.1Bass Manager, Tone Control, 12- Band Parametric EQ, Delay, 1:2 Upsampler
  - Microsoft® HDCD®
- Framework™ Applications for Download
  - Thomson MP3 Surround
  - Internal DSD-to-PCM Conversion
- Up to 12 Channels of 32-bit Serial Audio Input
- 6 Channel DSD Input
- 16 Ch x 32-bit PCM Out with either two 192 kHz S/PDIF Tx (144-pin package) or one 192 kHz S/PDIF Tx (128-pin package)
- Two SPI™/I²C®, One Parallel and One UART Port
- Customer Software Security Keys
- Large On-chip X, Y, and Program RAM & ROM
- SDRAM and Serial/Parallel Flash Memory Support

32-bit Audio Decoder DSP Family with Dual DSP Engine Technology

The CS4953xx DSP family are the enhanced versions of the CS495xx DSP family with higher overall performance and lower system cost. The CS4953xx includes all mainstream audio processing codes in on-chip ROM. This saves external memory for code storage. In addition, the intensive decoding tasks of Dolby Digital® Surround EX®, AAC multi-channel, DTS-ES 96/24, THX Ultra2 Cinema and Dolby Headphone can be accomplished without the expense of external SDRAM memory. With larger internal memories than the CS495xx, the CS49531x is designed to support up to 150 ms per channel of lip-sync delay. With 150 MHz internal clock speed, the CS4953xx supports the most demanding post-processing requirements. It is also designed for easy upgrading. Customers currently using the CS495xx can upgrade to the CS4953xx with minor hardware and software changes.

Ordering Information

See page 31 for ordering information



Preliminary Product Information This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. Documentation Strategy

The *CS4953xx Datasheet* describes the CS4953xx family of multichannel audio decoders. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS4953xx family of processors.

Table 1. CS4953xx Related Documentation

Document Name	Description
CS4953xx Datasheet	This document
CS4953xx Hardware User's Manual	Includes detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, Etc.
AN288 - CS4953xx Firmware User's Manual	Includes detailed firmware design information including signal processing flow diagrams and control API information

The scope of the *CS4953xx Datasheet* is primarily the hardware specifications of the CS4953xx family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS4953xx Data Sheet* is the system PCB designer, mcu programmer, and the quality control engineer.

2. Overview

The CS4953xx DSP Family, together with Cirrus Logic's comprehensive library of audio processing algorithms, enables the development of next-generation audio solutions. Cirrus Logic also provides a broad array of digital interface products, audio converters, and ARM® Processors to meet your audio system-level design requirements.

There are two devices in the CS4953xx DSP family. The CS495303 and CS495313 are differentiated by internal memory size and DSP Firmware. The CS495303 is available in a 128-pin QFP package and the CS495313 is available in either a 128-pin or 144-pin QFP package. The audio processing features of the CS495313 are a superset of audio features available in the CS495303. Please refer to Table 2 on page 6 for the speed and firmware features of each device.

2.1 Migrating from the CS495xx(2) to the CS4953xx

The CS4953xx was designed to provide an easy upgrade path from the CS495xx(2). Although 144-pin versions of the two devices are virtually identical with respect to external system connection, there are some small differences the hardware designer should be aware of:

- The PLL supply voltage on the CS4953xx is 3.3V vs. 1.8V on the CS495xx(2).
- The PLL filter topology is simpler when using the CS4953xx rather than the CS495xx(2).
- The CS4953xx adds support for 6-channel DSD input.
- The CS4953xx adds support for TDM mode on both audio input and output ports.
- The CS4953xx does not support external SRAM operation.
- The CS4953xx external SDRAM bus speed is fixed at 150 MHz vs. the 120 MHz max bus speed for the CS495xx(2). Some firmware modules also support a 75 MHz CS4953xx SDRAM bus speed. Please refer to AN288 for details.
- The CS4953xx CLKOUT pin can output XTALI or XTALI/2. The CS495xx(2) can only output XTALI.

2.2 Licensing

Licenses are required for all of the 3rd party audio decoding/processing algorithms listed below, including the application notes. Please contact your local Cirrus Sales representative for more information.

3. Code Overlays

The suite of software available for the CS4953xx family consists of an operating system (OS) and a library of overlays. The overlays have been divided into three main groups called Decoders, Mid-processors, and Post-processors. All software components are defined below:

1. OS/Kernel - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, error concealment, etc.

2. Decoders - Any Module that initially writes data into the audio I/O buffers, e.g. AC-3®, DTS, PCM, etc. All the decoding/processing algorithms listed below require delivery of PCM or IEC61937-packed, compressed data via I^2S- or LJ-formatted digital audio to the CS4953xx.

3. Mid-processors - Any module that processes audio I/O buffer PCM data in-place before the Post-processors. Generally speaking, these modules alter the number of valid channels in the audio I/O buffer through processes like Virtualization (n⇨2 channels) or Matrix Decoding (2⇨n channels). Examples are Dolby ProLogic IIx and DTS Neo:6.

4. Post-processors - Any module that processes audio I/O buffer PCM data in-place after the Mid-Processors. Examples are Bass Management, Audio Manager, Tone Control, EQ, Delay, Customer-specific Effects, Dolby Headphone/Virtual Speaker, etc.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new decoder is selected, the OS, mid-, and post-processors do not need to be reloaded — only the new decoder (the same is true for the other overlays).

Table 2 below lists the firmware available based on device selection. Please refer AN288 *CS4953xx Firmware User's Manual* for the latest listing of application codes and Cirrus Framework™ modules available.

Table 2. Device and Firmware Selection Guide[1]

Device	Pre-Process	Decode Processor A	Mid-processor A	Mid-processor B	Post-processor B
CS495303 **300 MIPS**	N/A	Stereo PCM Multi-Channel PCM (2:1 Down-sampling Option) Dolby Digital AAC MP3 HDCD	Dolby PLIIx Circle Surround® II (Stereo In) Cirrus Original Multi-Channel Surround (Effects / Reverb Processor) Down-mix (Simultaneous Process)	Dolby Headphone Dolby Virtual Speaker SRSTruSurround XT THX Select	APP (Advanced Post-processing) –Tone Control –Re-EQ –PEQ (up to 11 Bands) –Delay –7.1 Bass Manager –Audio Manager 1:2 Up-sampling
CS495313 ***(Superset of CS495303)*** **300 MIPS**	Lip Sync Delay	Same as CS495303 + DTS DTS-ES DTS 96/24	Same as CS495303 + DTS Neo:6 (Stereo In)	Same as CS495303 + THX Ultra2	

1. This feature list is a snapshot of features available as of the publication date of this revision of the data sheet. More features may now be available. Check with your Cirrus Logic Field Application Engineer (FAE) to obtain the latest feature list for the CS495303 and CS495313 products.

4. Hardware Functional Description

4.1 DSP Core

The CS4953xx is a dual-core DSP with separate X and Y data and P code memory spaces. Each core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two memory access control (MAC) operations per clock cycle. Each core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

Both DSP cores are coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the digital audio input (DAI) and digital audio output (DAO), external memory, or any DSP core memory, all without the intervention of the DSP. The DMA engine offloads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS4953xx functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS4953xx from a host mcu or external FLASH/EEPROM. Users can choose to use standard audio decoder and post-processor modules which are available from Cirrus Logic.

The CS4953xx is suitable for Audio Decoder, Audio Post-processor, Audio Encoder, DVD Audio/Video Player, and Digital Broadcast Decoder applications.

4.1.1 DSP Memory

Each DSP core has its own on-chip data and program RAM and ROM and does not require external memory for any of today's popular audio algorithms including Dolby Digital Surround EX, AAC Multichannel, DTS-ES 96/24, and THX Ultra2.

The memory maps for the DSPs are as follows. All memory sizes are composed of 32-bit words.

Table 3. CS495303 DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16k SRAM, 16k ROM	10k SRAM, 8k ROM
Y	16k SRAM, 32k ROM	16k SRAM, 16k ROM
P	8k SRAM, 32k ROM	8k SRAM, 24k ROM

Table 4. CS495313 DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16k SRAM, 16k ROM	10k SRAM, 8k ROM
Y	24k SRAM, 32k ROM	16k SRAM, 16k ROM
P	8k SRAM, 32k ROM	8k SRAM, 24k ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to 6 interrupt events, is programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The 12-channel (6 line) DAI port supports a wide variety of data input formats. The port is capable of accepting PCM, IEC61937, or DSD. Up to 32-bit word lengths are supported. Up to 6 channels of DSD are supported and internally converted to PCM before processing.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, which off-loads the task of monitoring the S/PDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

There are two DAO ports. Each port can output 8 channels of up to 32-bit PCM data. The port supports data rates from 32 kHz to 192 kHz. Each port can be configured as an independent clock domain in slave mode, or the ratio of the two clocks can be set to even multiples of each other in master mode. The two ports can also be ganged together into a single clock domain. Each port has one serial audio pin that can be configured as a 192 kHz S/PDIF transmitter (data with embedded clock on a single line).
Note: Only one S/PDIF transmitter pin is available in the 128-pin package.

4.2.3 Serial Control Port 1 & 2 (I^2C® or SPI™)

There are two on-chip serial control ports that are capable of operating as master or slave in either I^2C or SPI modes. SCP1 defaults to slave operation. It is dedicated for external host-control and supports an external clock up to 50 MHz in SPI mode. It is present in both the 144- and 128-pin packages. This high clock speed enables very fast code download, control or data delivery. SCP2 defaults to master mode and is dedicated for booting from external serial Flash memory or for audio sub-system control. SCP2 does not include the SCP2_BSY# pin in the 128-pin package.

4.2.4 Parallel Control Port

The CS4953xx parallel port supports both Motorola® and Intel® interfaces. It can be used for both control and data delivery. The parallel port pins are multiplexed with serial control port 2 and are available in the 144-pin package.

4.2.5 External Memory Interface

The external memory interface controller supports up to 128 Mbits of SDRAM, using a 16-bit data bus. The memory controller supports up to 1 MB of Flash memory in 8-bit data bus-width mode or 2 MB in 16-bit data bus-width mode.

4.2.6 GPIO

Many of the CS4953xx peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.7 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS4953xx defaults to running from the external reference frequency and can be switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external serial FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS4953xx pins are multi-functional. For details on pin functionality please refer to the *CS4953xx Hardware User's Manual*.

4.3.2 Termination Requirements

Open-drain pins on the CS4953xx must be pulled high for proper operation. Please refer to the *CS4953xx Hardware User's Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on the CS4953xx are used to select the boot mode upon the rising edge of reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS4953xx Hardware User's Manual*.

4.3.3 Pads

The CS4953xx I/O operates from the 3.3 V supply and is 5V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device.

5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25 °C, C_L = 20 pF, VDD = VDDA = 1.8 V, VDDIO = 3.3 V, GNDD = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Max	Unit
DC power supplies: Core supply	VDD	–0.3	2.0	V
PLL supply	VDDA	–0.3	3.6	V
I/O supply	VDDIO	–0.3	3.6	V
|VDDA – VDDIO|		-	0.3	V
Input pin current, any pin except supplies	I_{in}	-	+/- 10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on I/O pins	V_{inio}	-0.3	5.0	V
Storage temperature	T_{stg}	–65	150	°C

CAUTION: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GNDD = GNDIO = GNDA = 0 V; all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies: Core supply	VDD	1.71	1.8	1.89	V
PLL supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
|VDDA – VDDIO|			0		V
Ambient operating temperature	T_A		-		°C
- CQ		0		+ 70	
- DQ		- 40		+ 85	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTI	V_{IL}	-	-	0.8	V
Low-level input voltage, XTI	V_{ILXTI}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage (I_O = -4mA), except XTI, SDRAM pins	V_{OH}	VDDIO * 0.9	-	-	V
Low-level output voltage (I_O = 4mA), except XTI, SDRAM pins	V_{OL}	-	-	VDDIO * 0.1	V
SDRAM High-level output voltage (I_O = -8mA)	V_{OH}	VDDIO * 0.9	-	-	V
SDRAM Low-level output voltage (I_O = 8mA)	V_{OL}	-	-	VDDIO * 0.1	V
Input leakage current (all digital pins with internal pull-up resistors disabled)	I_{IN}	-	-	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)	I_{IN-PU}	-	-	50	µA

5.4 Power Supply Characteristics

(measurements performed under operating conditions)

Parameter	Min	Typ	Max	Unit
Power supply current:				
Core and I/O operating: VDD[1]	-	500	-	mA
PLL operating: VDDA	-	3.5	-	mA
With external memory and most ports operating: VDDIO	-	120	-	mA

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (144 LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		-	48	-	
Four-layer Board[2]		-	40	-	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		-	.39	-	
Four-layer Board[2]		-	.33	-	

5.6 Thermal Data (128 LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		-	53	-	
Four-layer Board[2]		-	44	-	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		-	.45	-	
Four-layer Board[2]		-	.39	-	

Notes:
1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20 % of the top & bottom layers.
2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20 % of the top & bottom layers and 0.5-oz copper covering 90 % of the internal power plane and ground plane layers.
3. To calculate the die temperature for a given power dissipation
4. T_j = Ambient Temperature + [(Power Dissipation in Watts) * θ_{ja}]
5. To calculate the case temperature for a given power dissipation
6. $T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

5.7 Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
RESET# minimum pulse width low	T_{rstl}	1	-	µs
All bidirectional pins high-Z after RESET# low	T_{rst2z}	-	100	ns
Configuration pins setup before RESET# high	T_{rstsu}	50	-	ns
Configuration pins hold after RESET# high	T_{rsthld}	20	-	ns

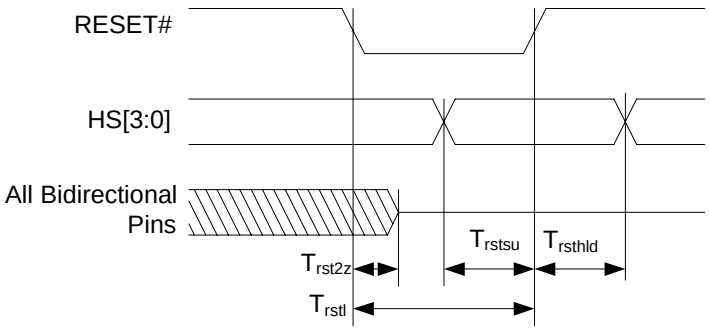

Figure 1. RESET Timing

5.8 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	11.2896	27	MHz
XTI period	T_{clki}	33.3	100	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR		50	W

1. Part characterized with the following crystal frequency values: 11.2896, 12.288, 18.432, 24.576, & 27 MH.z.
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

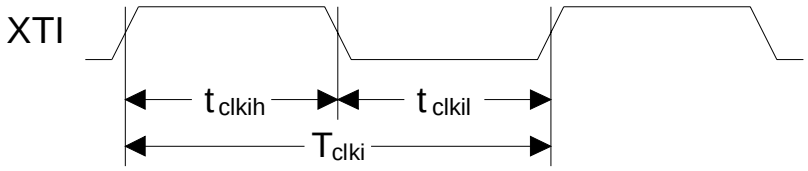

Figure 2. XTI Timing

5.9 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency[1]	F_{dclk}	-		MHz
CS49530x-CVZ		F_{xtal}	150	
CS49531x-CQZ		F_{xtal}	150	
CS49531x-CVZ		F_{xtal}	150	
CS49530x-DVZ		F_{xtal}	TBD	
CS49531x-DQZ		F_{xtal}	TBD	
CS49531x-DVZ		F_{xtal}	TBD	
Internal DCLK period[1]	DCLKP	-		ns
CS49530x-CVZ		6.7	$1/F_{xtal}$	
CS49531x-CQZ		6.7	$1/F_{xtal}$	
CS49531x-CVZ		6.7	$1/F_{xtal}$	
CS49530x-DVZ		TBD	$1/F_{xtal}$	
CS49531x-DQZ		TBD	$1/F_{xtal}$	
CS49531x-DVZ		TBD	$1/F_{xtal}$	

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.10 Switching Characteristics — Serial Control Port - SPI Slave Mode.

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		25	MHz
SCP_CS# falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		11	ns
SCP_CLK falling to SCP_IRQ# rising	$t_{spiirqh}$	-		20	ns
SCP_CS# rising to SCP_IRQ# falling	$t_{spiirql}$	0			ns
SCP_CLK low to SCP_CS# rising	t_{spicsh}	24		-	ns
SCP_CS# rising to SCP_MISO output high-Z	$t_{spicsdz}$	-	20		ns
SCP_CLK rising to SCP_BSY# falling	$t_{spicbsyl}$	-	3*DCLKP+20		ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY# pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.

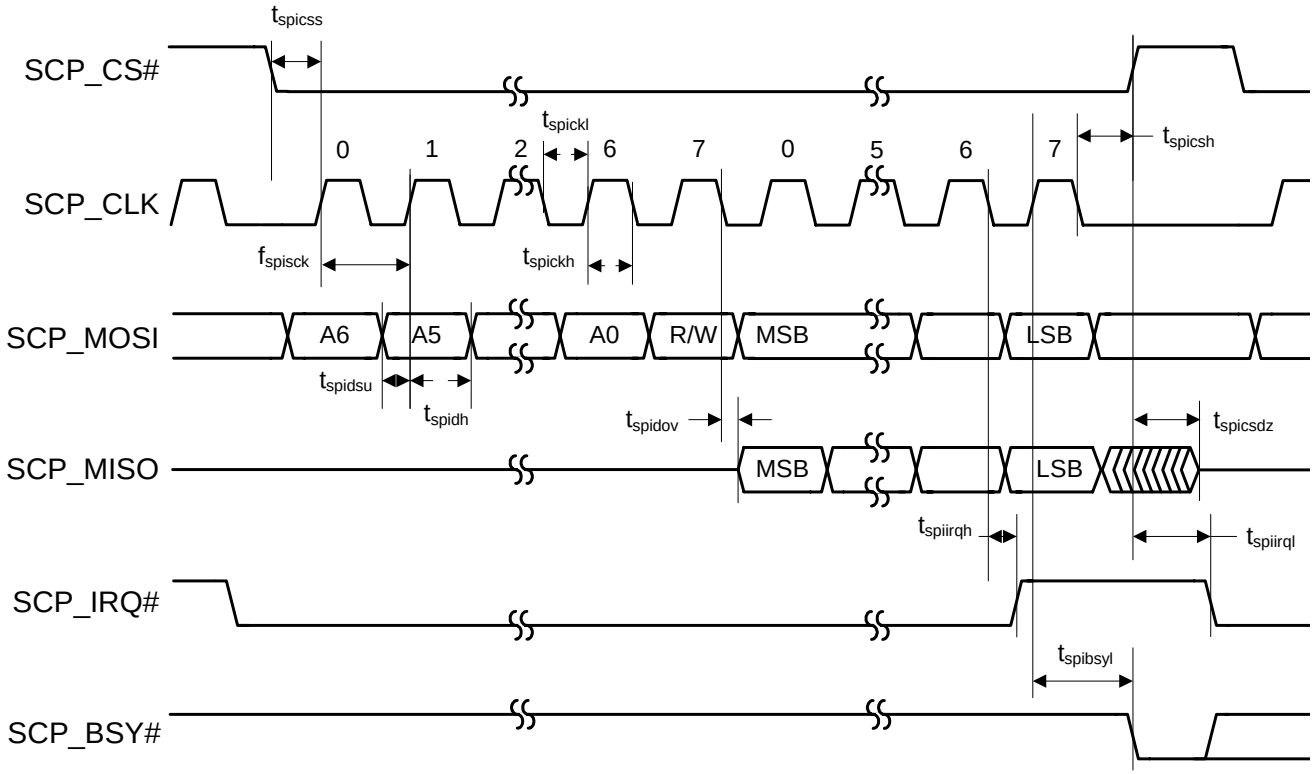

Figure 3. Serial Control Port - SPI Slave Mode Timing

5.11 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{spisck}	-		$F_{xtal}/2^2$	MHz
SCP_CS# falling to SCP_CLK rising [3]	t_{spicss}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
SCP_CLK low time	t_{spickl}	18		-	ns
SCP_CLK high time	t_{spickh}	18		-	ns
Setup time SCP_MISO input	t_{spidsu}	11		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		11	ns
SCP_CLK low to SCP_CS# falling	t_{spicsl}	7		-	ns
SCP_CLK low to SCP_CS# rising	t_{spicsh}	-	11*DCLKP + (SCP_CLK PERIOD)/2	-	ns
Bus free time between active SCP_CS#	t_{spicsx}		3*DCLKP	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.8.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

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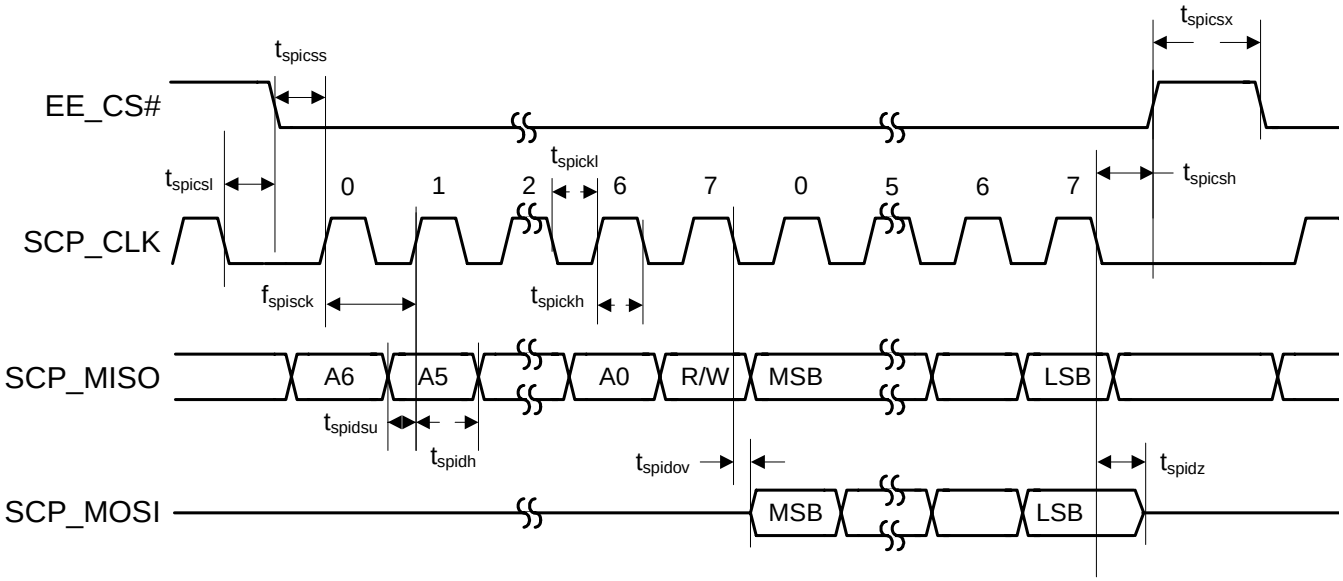


Figure 4. Serial Control Port - SPI Master Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-		400	kHz
SCP_CLK low time	t_{iicckl}	1.25		-	µs
SCP_CLK high time	t_{iicckh}	1.25		-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25		-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3		-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to SCP_IRQ# rising	$t_{iicirqh}$	-		3∗DCLKP + 40	ns
NAK condition to SCP_IRQ# low	$t_{iicirql}$		3∗DCLKP + 20		ns
SCP_CLK rising to SCB_BSY# low	$t_{iicbsyl}$	-	3∗DCLKP + 20		ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY# pin should be implemented to prevent overflow of the input data buffer.

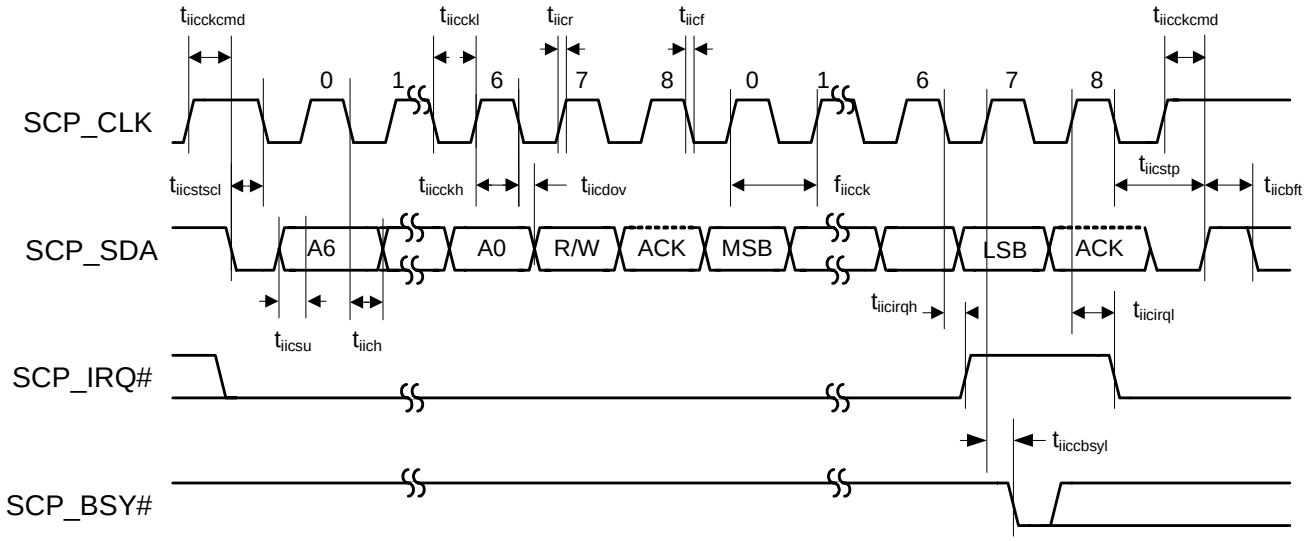


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.13 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	-	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	-	µs
SCP_CLK high time	t_{iicckh}	1.25	-	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	-	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	-	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

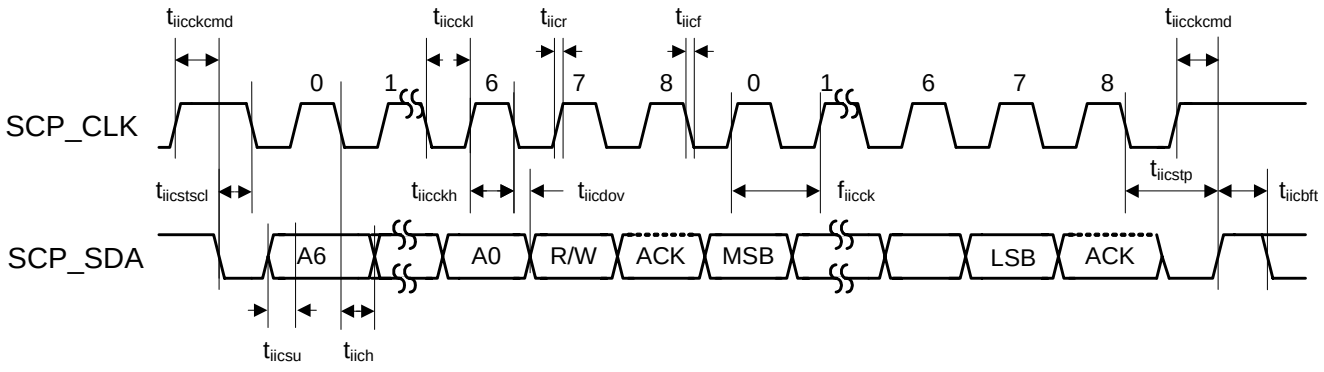


Figure 6. Serial Control Port - I²C Master Mode Timing

5.14 Switching Characteristics — Parallel Control Port - Intel® Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before PCP_CS# and PCP_RD# low or PCP_CS# and PCP_WR# low	t_{ias}	5		-	ns
Address hold time after PCP_CS# and PCP_RD# low or PCP_CS# and PCP_WR# high	t_{iah}	5		-	ns
Read					
Delay between PCP_RD# then PCP_CS# low or PCP_CS# then PCP_RD# low	t_{icdr}	0		-	ns
Data valid after PCP_CS# and PCP_RD# low	t_{idd}	-		18	ns
PCP_CS# and PCP_RD# low for read	t_{irpw}	24		-	ns
Data hold time after PCP_CS# or PCP_RD# high	t_{idhr}	8		-	ns
Data high-Z after PCP_CS# or PCP_RD# high	t_{idis}	-		18	ns
PCP_CS# or PCP_RD# high to PCP_CS# and PCP_RD# low for next read[1]	t_{ird}	30		-	ns
PCP_CS# or PCP_RD# high to PCP_CS# and PCP_WR# low for next write[1]	t_{irdtw}	30		-	ns
PCP_RD# rising to PCP_IRQ# rising	$t_{irdirqhl}$	-		12	ns
Write					
Delay between PCP_WR# then PCP_CS# low or PCP_CS# then PCP_WR# low	t_{icdw}	0		-	ns
Data setup before PCP_CS# or PCP_WR# high	t_{idsu}	8		-	ns
PCP_CS# and PCP_WR# low for write	t_{iwpw}	24		-	ns
Data hold after PCP_CS# or PCP_WR# high	t_{idhw}	8		-	ns
PCP_CS# or PCP_WR# high to PCP_CS# and PCP_RD# low for next read[1]	t_{iwtrd}	30		-	ns
PCP_CS# or PCP_WR# high to PCP_CS# and PCP_WR# low for next write[1]	t_{iwd}	30		-	ns
PCP_WR# rising to PCP_BSY# falling	$t_{iwrbsyl}$	-	2*DCLKP + 20	-	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY# pin/bit should be observed to prevent overflowing the input data buffer. AN288 *CS4953xx Firmware Uses's Manual* should be consulted for the firmware speed limitations.

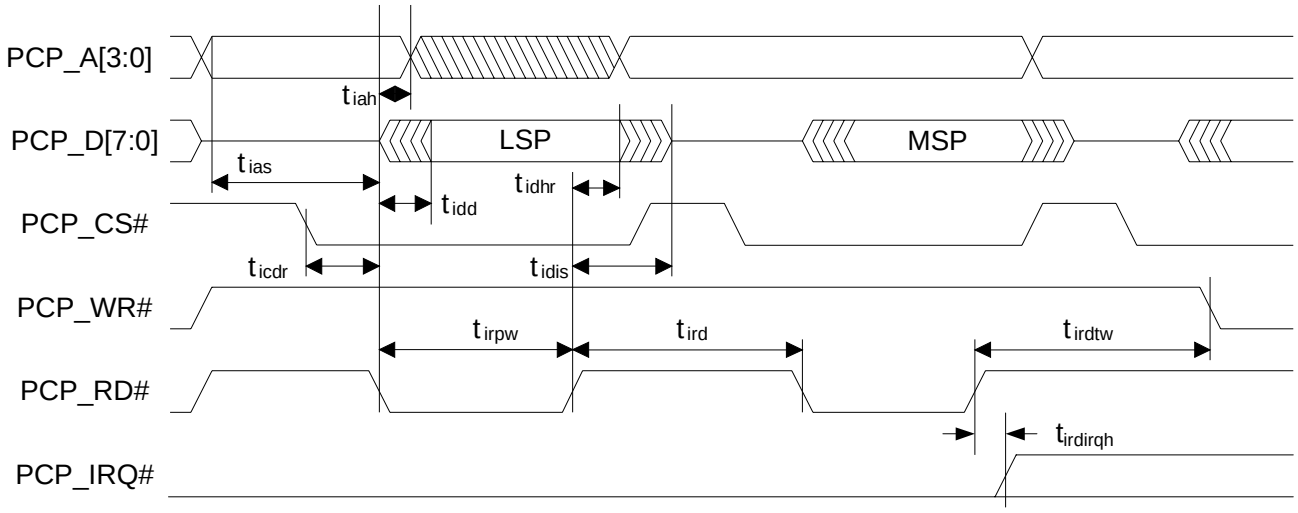


Figure 7. Parallel Control Port - Intel® Mode Read Cycle

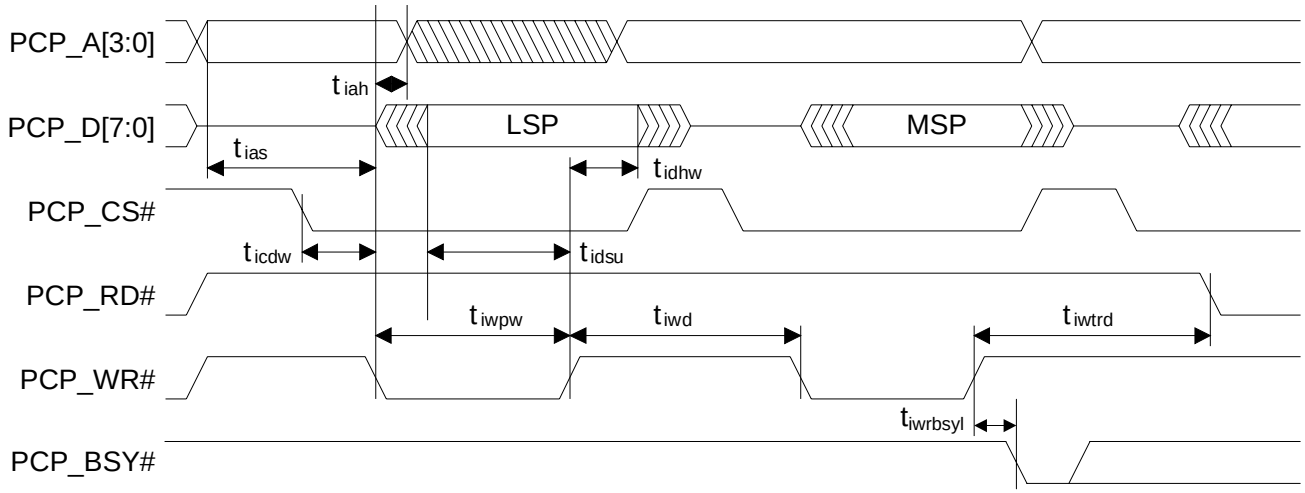


Figure 8. Parallel Control Port - Intel Mode Write Cycle

5.15 Switching Characteristics — Parallel Control Port - Motorola® Slave Mode

Parameter	Symbol	Min		Max	Unit
Address setup before PCP_CS# and PCP_DS# low	t_{mas}	5		-	ns
Address hold time after PCP_CS# and PCP_DS# low	t_{mah}	5		-	ns
Read					
Delay between PCP_DS# then PCP_CS# low or PCP_CS# then PCP_DS# low	t_{mcdr}	0		-	ns
Data valid after PCP_CS# and PCP_DS# low with PCP_R/W# high	t_{mdd}	-		19	ns
PCP_CS# and PCP_DS# low for read	t_{mrpw}	24		-	ns
Data hold time after PCP_CS# or PCP_DS# high after read	t_{mdhr}	8		-	ns
Data high-Z after PCP_CS# or PCP_DS# high after read	t_{mdis}	-		18	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low for next read[1]	t_{mrd}	30		-	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low for next write[1]	t_{mrdtw}	30		-	ns
PCP_RW# rising to PCP_IRQ# falling	$t_{mrwirqh}$	-		12	ns
Write					
Delay between PCP_DS# then PCP_CS# low or PCP_CS# then PCP_DS# low	t_{mcdw}	0		-	ns
Data setup before PCP_CS# or PCP_DS# high	t_{mdsu}	8		-	ns
PCP_CS# and PCP_DS# low for write	t_{mwpw}	24		-	ns
PCP_R/W# setup before PCP_CS# AND PCP_DS# low	t_{mrwsu}	24		-	ns
PCP_R/W# hold time after PCP_CS# or PCP_DS# high	t_{mrwhld}	8		-	ns
Data hold after PCP_CS# or PCP_DS# high	t_{mdhw}	8		-	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low with PCP_R/W# high for next read[1]	t_{mwtrd}	30		-	ns
PCP_CS# or PCP_DS# high to PCP_CS# and PCP_DS# low for next write[1]	t_{mwd}	30		-	ns
PCP_RW# rising to PCP_BSY# falling	$t_{mrwbsyl}$	-	2*DCLKP + 20	-	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY# pin/bit should be observed to prevent overflowing the input data buffer. AN288 *CS4953xx Firmware Uses's Manual* should be consulted for the firmware speed limitations.

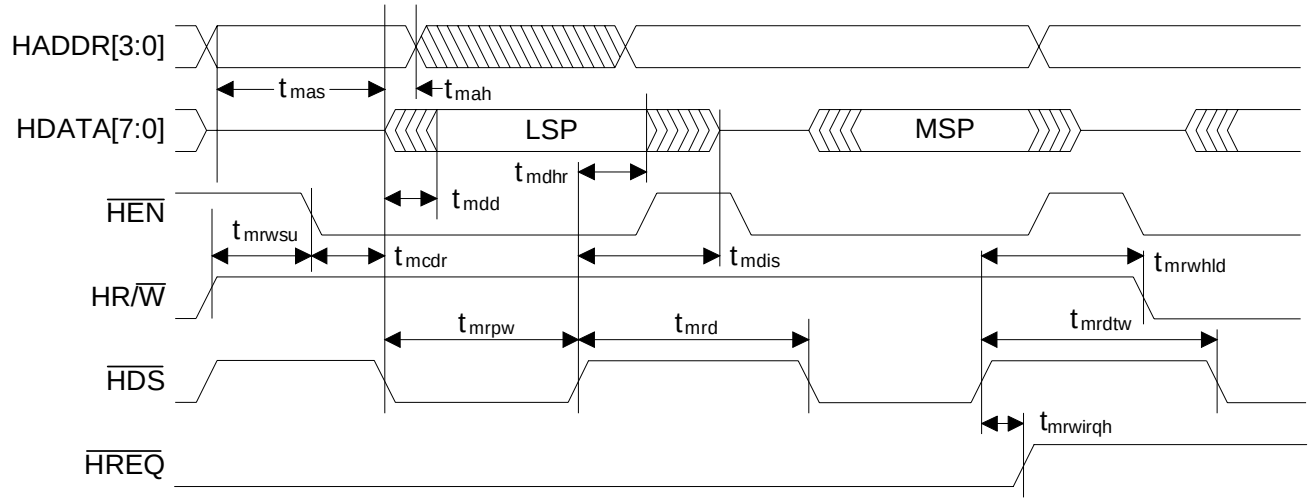


Figure 9. Parallel Control Port - Motorola® Mode Read Cycle Timing

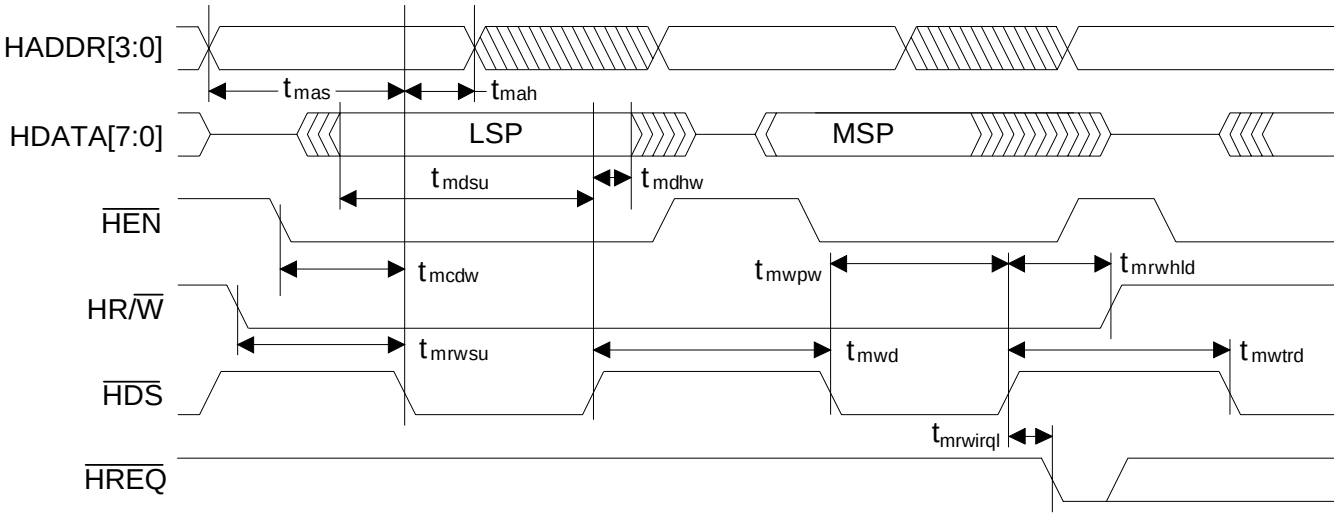


Figure 10. Parallel Control Port - Motorola Mode Write Cycle Timing

5.16 Switching Characteristics — UART

Parameter	Symbol	Min	Max	Unit
UART_CLK period[1]	t_{uclki}	266	-	ns
UART_CLK duty cycle	-	40	60	%
Setup time for UART_RXD	$t_{uckrxsu}$	5	-	
Hold time for UART_RXD	$t_{uckrxdv}$	5	-	ns
Delay from CLK transition to TXD transition	$t_{ucktxdv}$	-	29	ns
	t_{txen}	?	?	ns
	t_{txhz}	?	?	ns

1. The minimum clock period is limited to DCLKP/32 or the minimum value, whichever is larger.

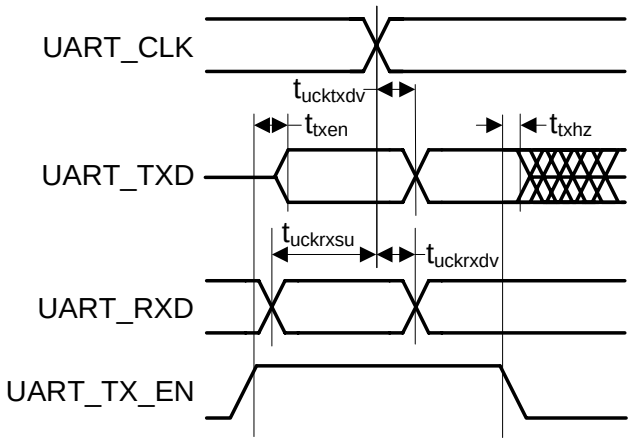


Figure 11. UART Timing

5.17 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	10	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

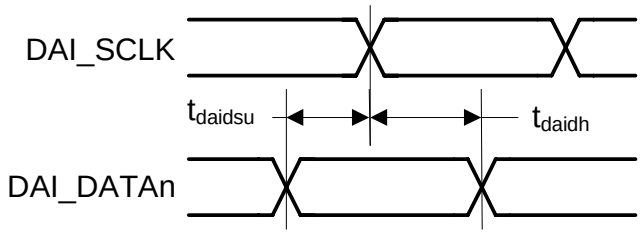


Figure 12. Digital Audio Input (DAI) Port Timing Diagram

5.18 Switching Characteristics — DSD Slave Input Port

Parameter	Symbol	Min	Typ	Max	Unit
DSD_SCLK Pulse Width Low	t_{sclkl}	78	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	78	-	-	ns
DSD_SCLK Frequency (64x Oversampled)	-	1.024	-	3.2	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns
DSD clock to data transition (Phase Modulation mode)	t_{dpm}	-20	-	20	ns

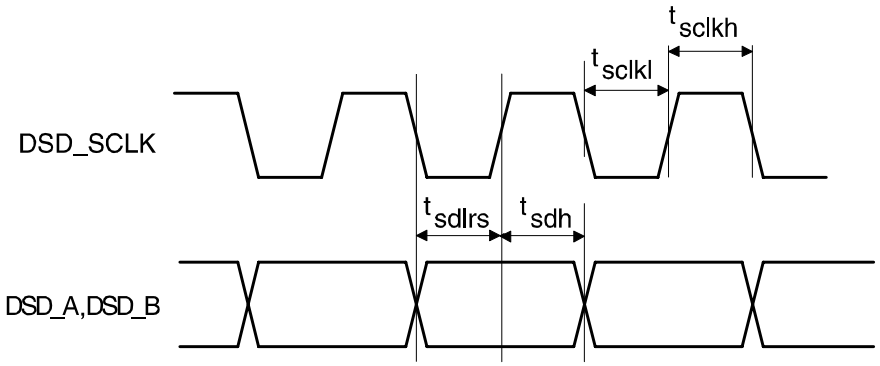


Figure 13. Direct Stream Digital - Serial Audio Input Timing

5.19 Switching Characteristics — Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period[1]	$T_{daomclk}$	40	-	ns
DAO_MCLK duty cycle[1]	-	40	60	%
DAO_SCLK period for Master or Slave mode[2]	$T_{daosclk}$	40	-	ns
DAO_SCLK duty cycle for Master or Slave mode[2]	-	40	60	%
Master Mode (Output A1 Mode)[2,3]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively[4]	$t_{daomstlr}$	-	8	ns
DAO_DATA[3:0] delay from DAO_SCLK transition[4]	t_{daomdv}	-	10	ns
Slave Mode (Output A0 Mode)[5]				
DAO_DATA[3..0] delay from DAO_SCLK transition[4]	t_{daosdv}		15	ns

1. CS4953xx has two Digital Audio Output modules having similar signal names ending in 1 and 2. Both DAO ports share a common MCLK but have independent SCLKs and LRCLKs.
2. Master mode timing specifications are characterized, not production tested.
3. Master mode is defined as the CS4953xx driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
4. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.

5.Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.

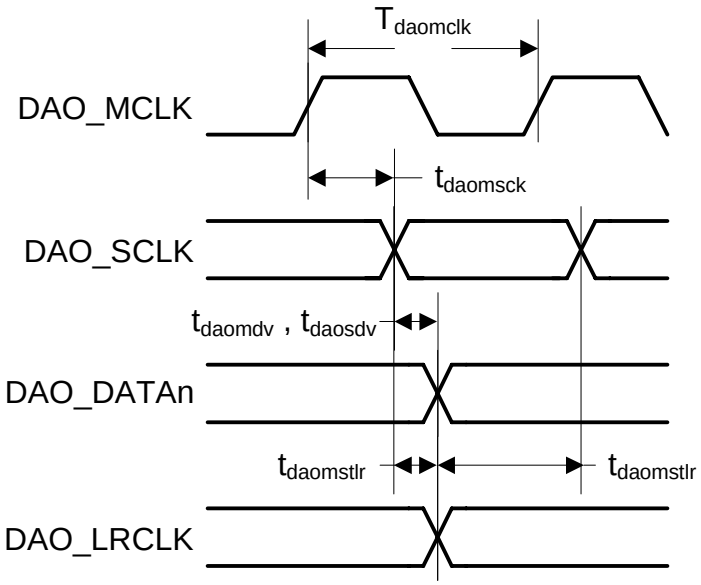


Figure 14. Digital Audio Port Timing, MCLK Master Mode

5.20 Switching Characteristics — External Memory Interface - Flash Mode

Parameter	Symbol	Min	Max	Unit
Write Cycle				
Address Setup time to EXT_WE# falling	t_{xmwasu}	1.2 * DCLKP		ns
EXT_CS# falling to EXT_WE# falling[1]	t_{xmcswe}	(Flash_WEN_CYCLE + 1.2) * DCLKP		ns
EXT_CS# falling to EXT_WE# rising[1]	t_{xmcswa}	(Flash_WR_CYCLE + 2.2) * DCLKP		ns
EXT_WE# low time	t_{xmwp}	2.2 * DCLKP		ns
Data Hold after EXT_WE# or EXT_CS# high	t_{xmwdh}	0.9 * DCLKP		ns
Address Hold from end of write	t_{xmwah}	0.8 * DCLKP		ns
EXT_WE# falling to data valid	t_{xmwedv}	-	0	ns
EXT_CS# high time[2]	t_{xmcsh}	TBD		ns
Read Cycle				
Single Word Read Cycle[1]	t_{xmrdc}	(Flash_RD_CYCLE + 1) * DCLKP		ns
EXT_CS# falling to EXT_OE# falling[1]	t_{xmcsoe}	Flash_OEN_CYCLE * DCLKP + 1		ns
Data Hold after EXT_OE# or EXT_CS# high	t_{xmrdh}	4		ns
Data Input Setup Time	t_{xmrdsu}	7		ns
Bus Turnaround Cycle Delay, Read to Write Cycle or Static to Dynamic[1, 3]	t_{xmturn}	(Flash_TURN_CYCLE + 1) * DCLKP		ns

1. The following parameters are set by communication with the application firmware. Please refer to AN288 or *CS4953xx Firmware Users Manual* for more information.
   0 < Flash_WEN_CYCLE < 15
   0 < Flash_WR_CYCLE < 31
   1 < Flash_RD_CYCLE < 31
   0 < Flash_OEN_CYCLE < 15
   4 < Flash_TURN_CYCLE < 15
2. A data write transaction is either a burst of two 16-bit half words or four 8-bit bytes with EXT_CS# toggling between address phases.
3. A data read transaction is either a burst of two 16-bit half words (as shown) or four 8-bit bytes with EXT_CS# remaining asserted between address phases.

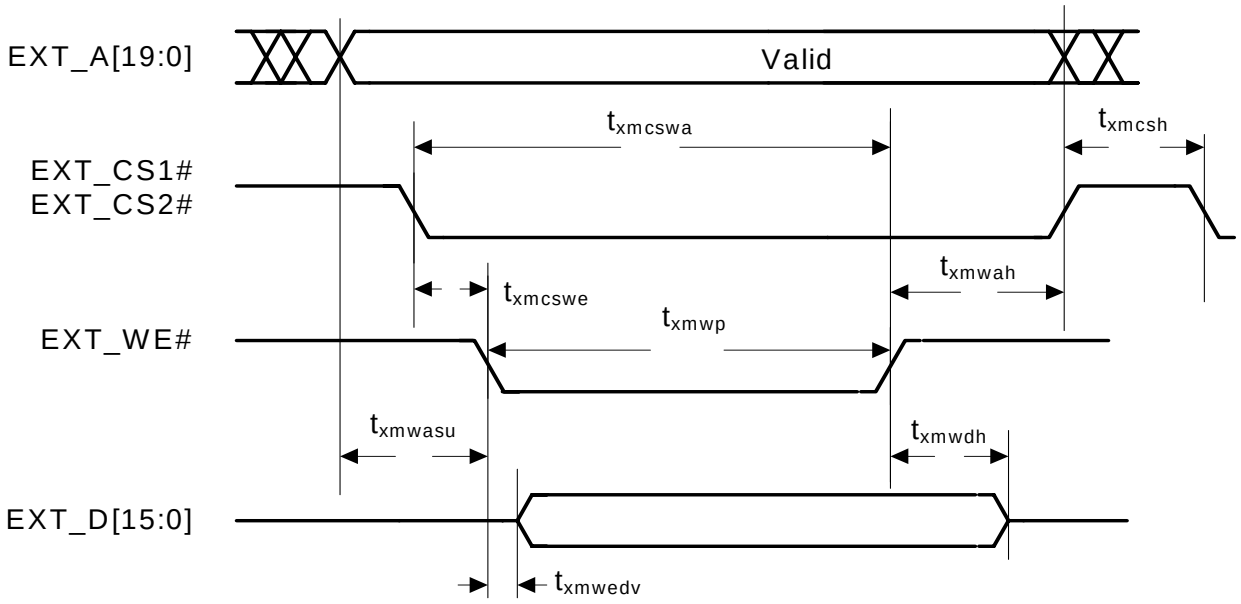


Figure 15. External Memory Interface - Flash Write Cycle Timing

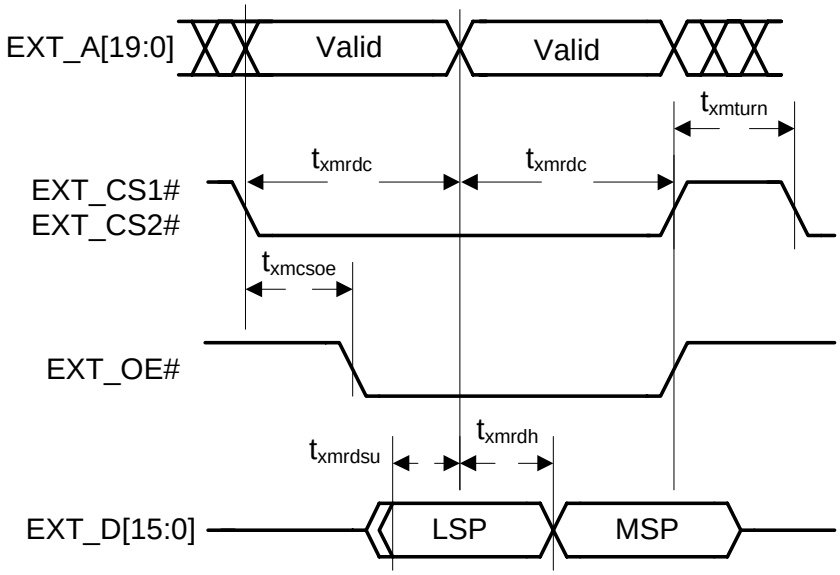


Figure 16. External Memory Interface - Flash Read Cycle Timing

5.21 Switching Characteristics — SDRAM Interface

Refer to Figure 17 through Figure 20.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3		-	ns
SD_CLKIN low time	t_{sdclkl}	2.3		-	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	-		1	ns
SD_CLKOUT Frequency			150		MHz
SD_CLKOUT duty cycle	-	45		55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	-		3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}		1.1	-	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	-	3.8	-	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38		-	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3		-	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	1.38		-	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	-	3.8	-	ns

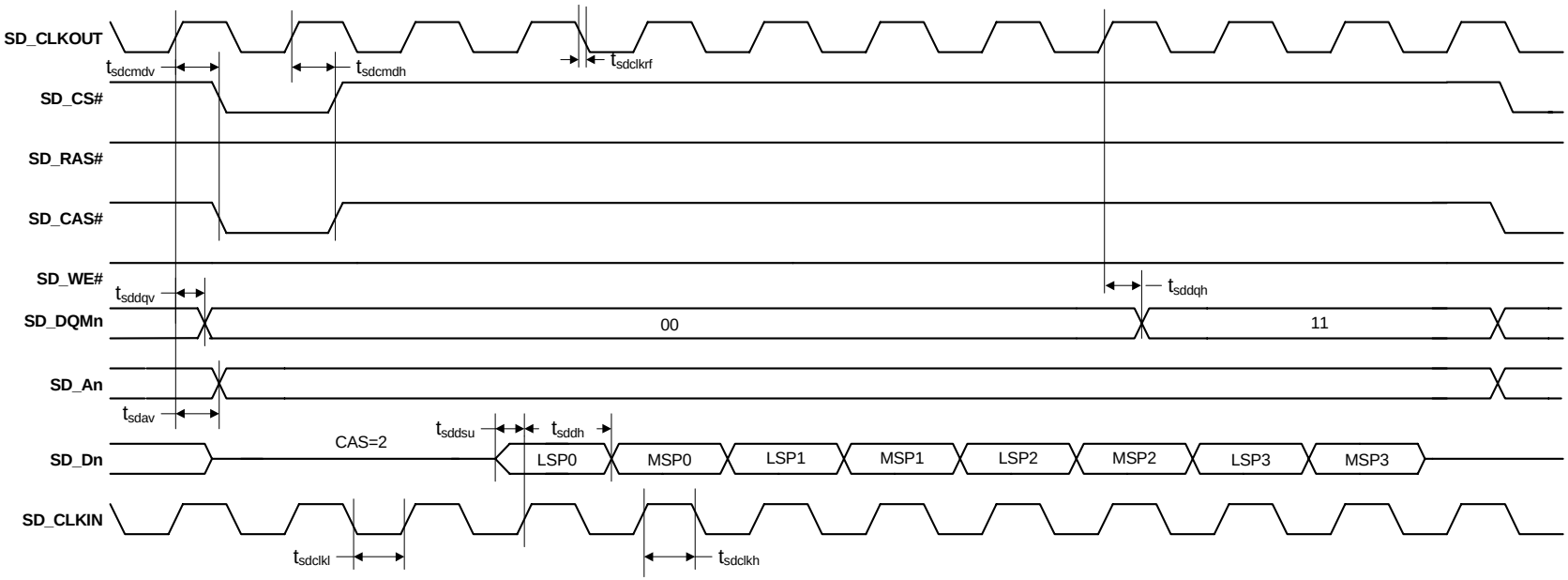


Figure 17. External Memory Interface - SDRAM Burst Read Cycle

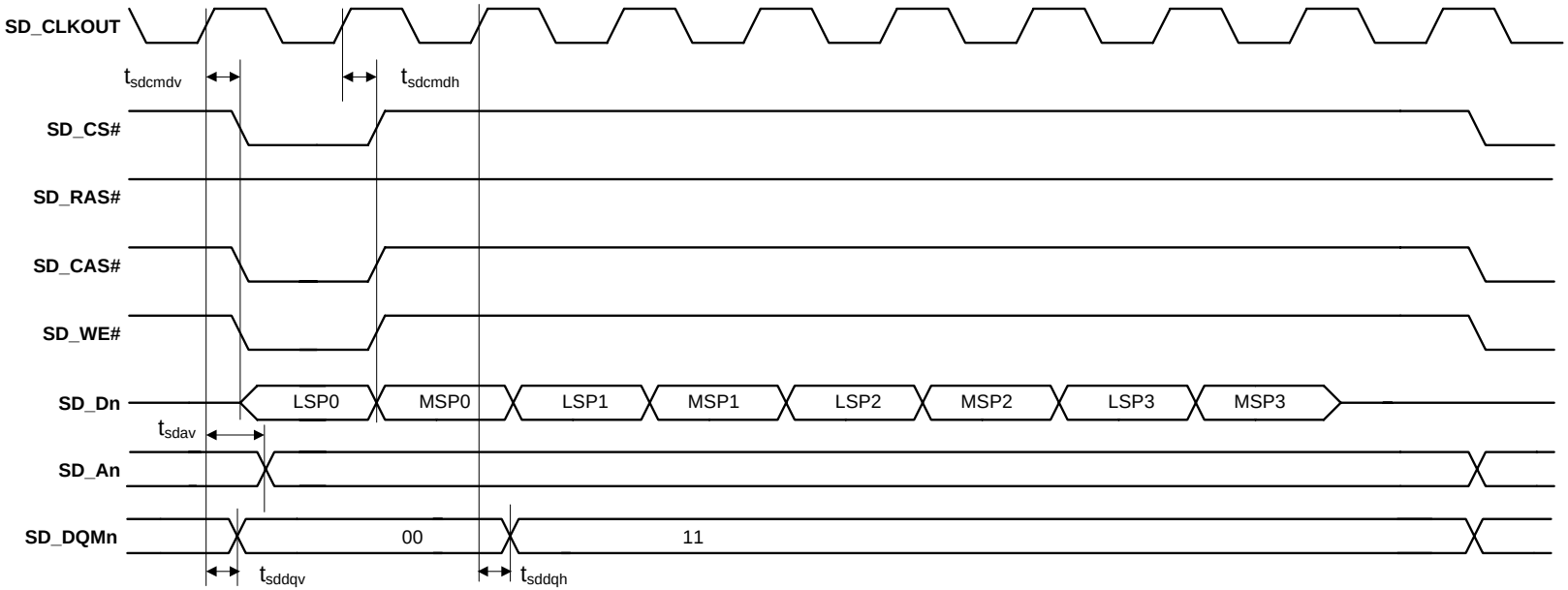


Figure 18. External Memory Interface - SDRAM Burst Write Cycle

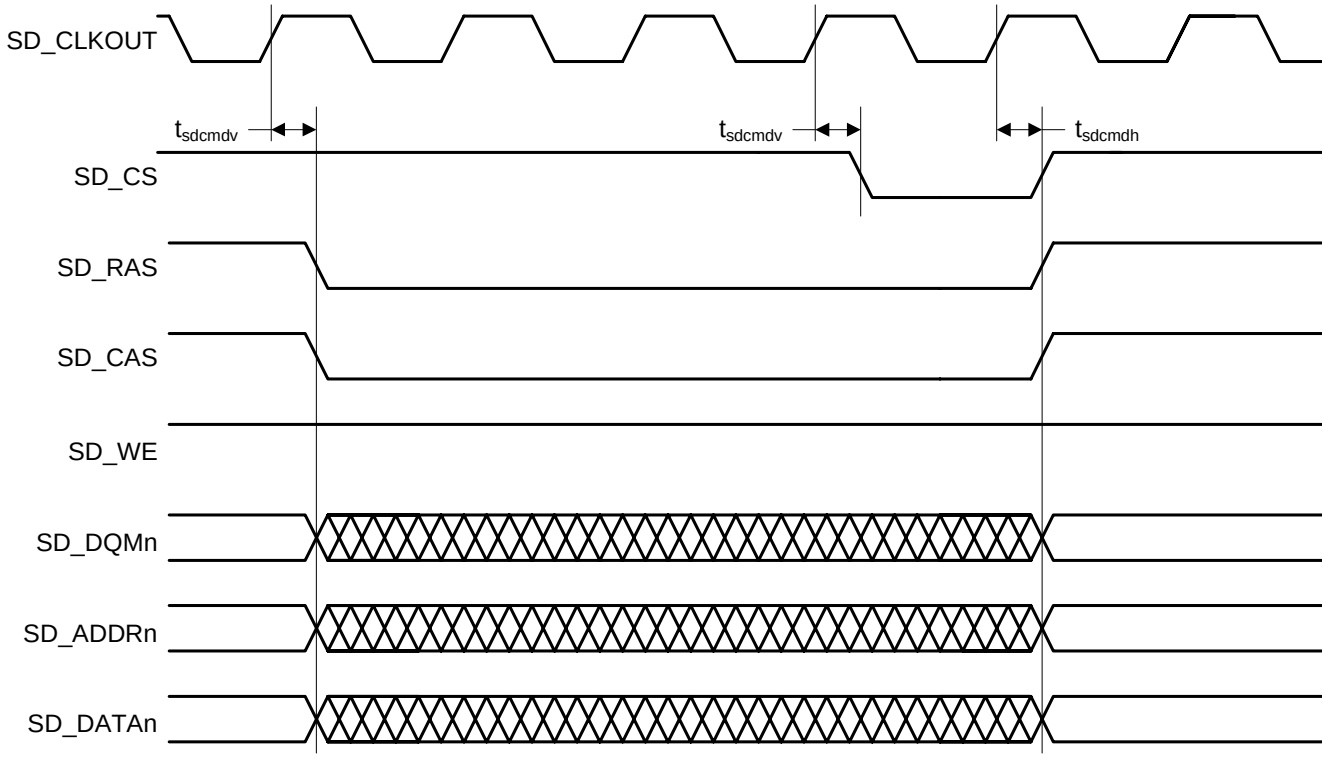


Figure 19. External Memory Interface - SDRAM Auto Refresh Cycle

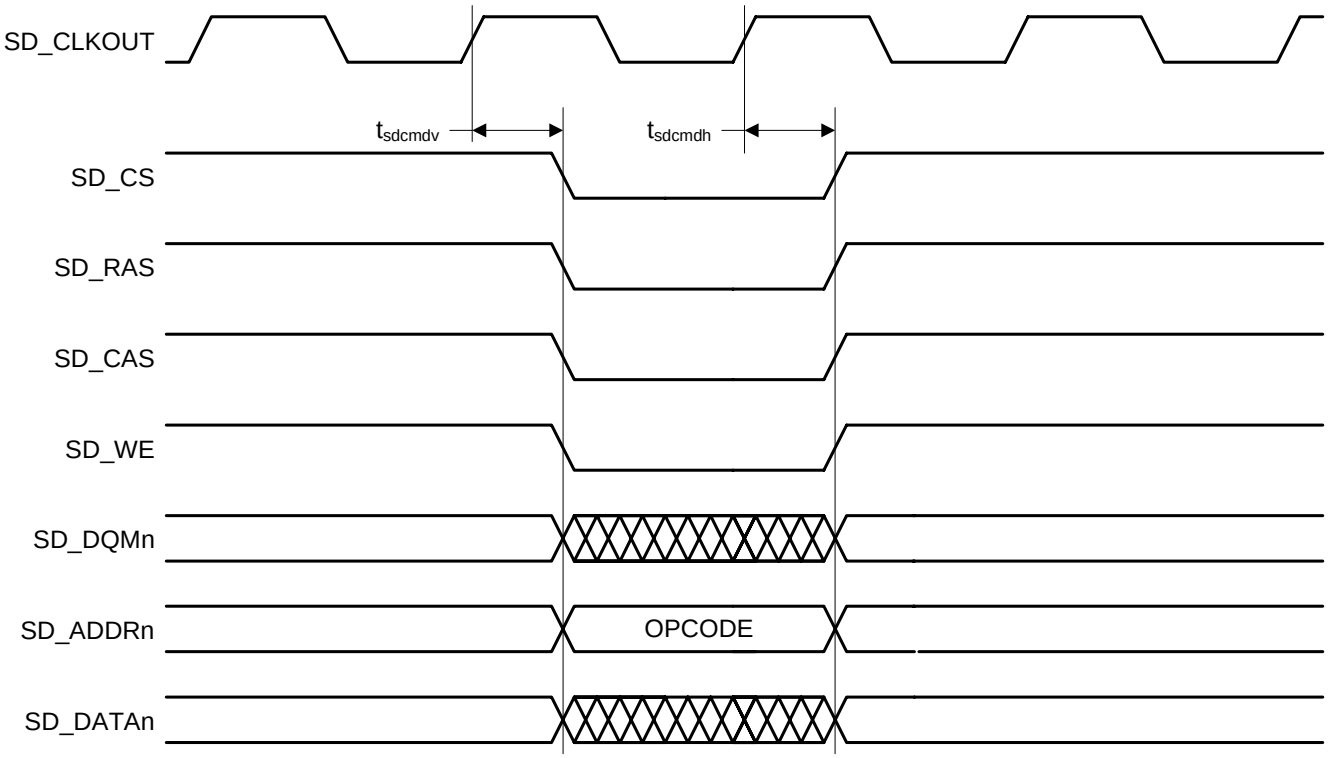


Figure 20. External Memory Interface - SDRAM Load Mode Register Cycle

6. Ordering Information

The CS4953xx family part number is described as follows:

CS495NNI-XYZ

where

NN - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 5. Ordering Information

Part No.	Grade	Temp. Range	Package
CS495303-CVZ	Commercial	0 to +70 °C	128-pin LQFP
CS495303-DVZ	Automotive	-40 to +85 °C	
CS495313-CQZ	Commercial	0 to +70 °C	144-pin LQFP
CS495313-DQZ	Automotive	-40 to +85 °C	
CS495313-CVZ	Commercial	0 to +70 °C	128-pin LQFP
CS495313-DVZ	Automotive	-40 to +85 °C	

Note: Please contact the factory for availability of the -D (automotive grade) package.

7. Environmental, Manufacturing, & Handling Information

Table 6. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS495303-CVZ	260 °C	3	7 Days
CS495303-DVZ			
CS495313-CQZ			
CS495313-DQZ			
CS495313-CVZ			
CS495313-DVZ			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. Device Pinout Diagrams

8.1 128-Pin LQFP Pinout Diagram

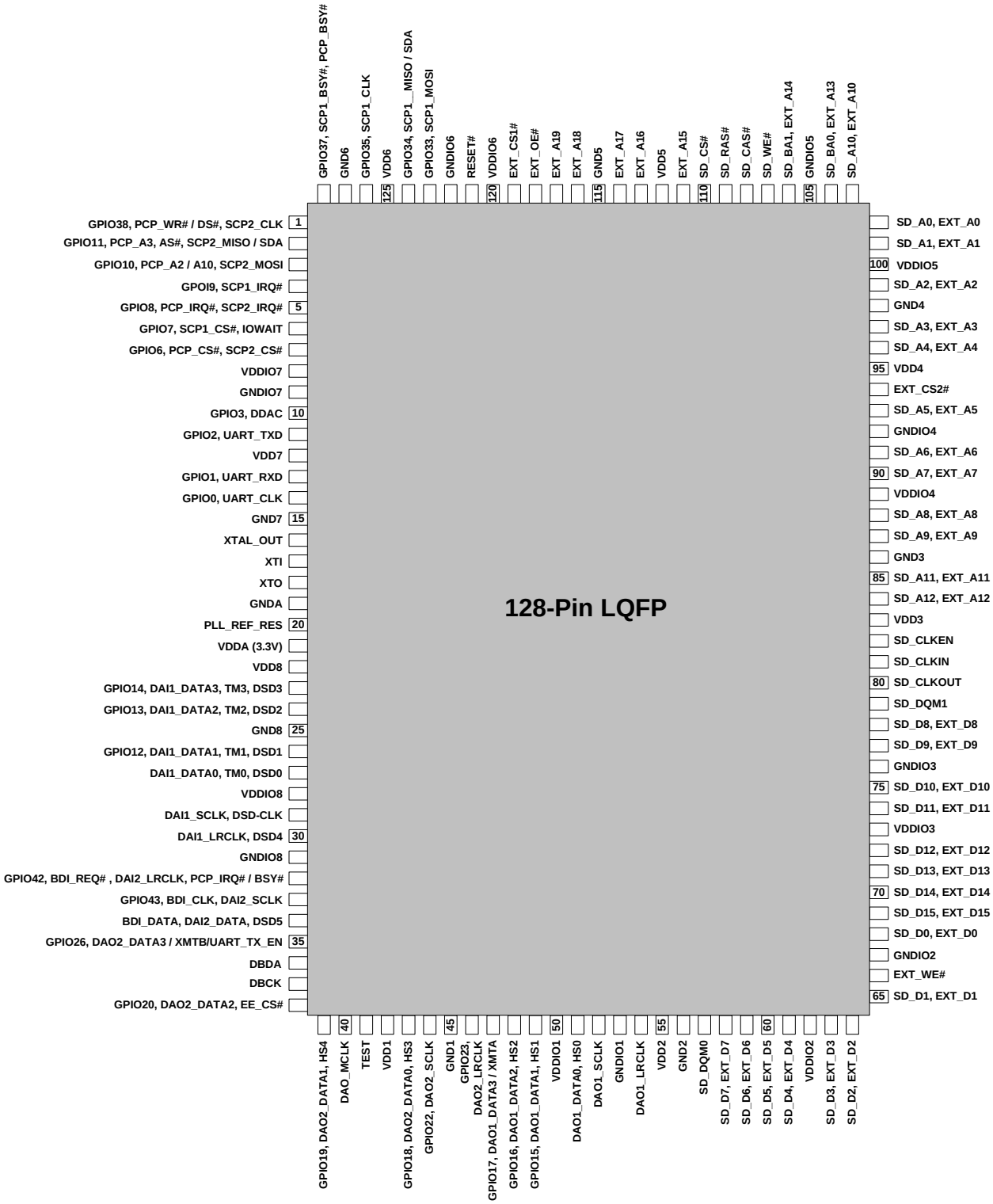


Figure 21. 128-Pin LQFP Pin-Out Drawing

8.2 144-Pin LQFP Pinout Diagram

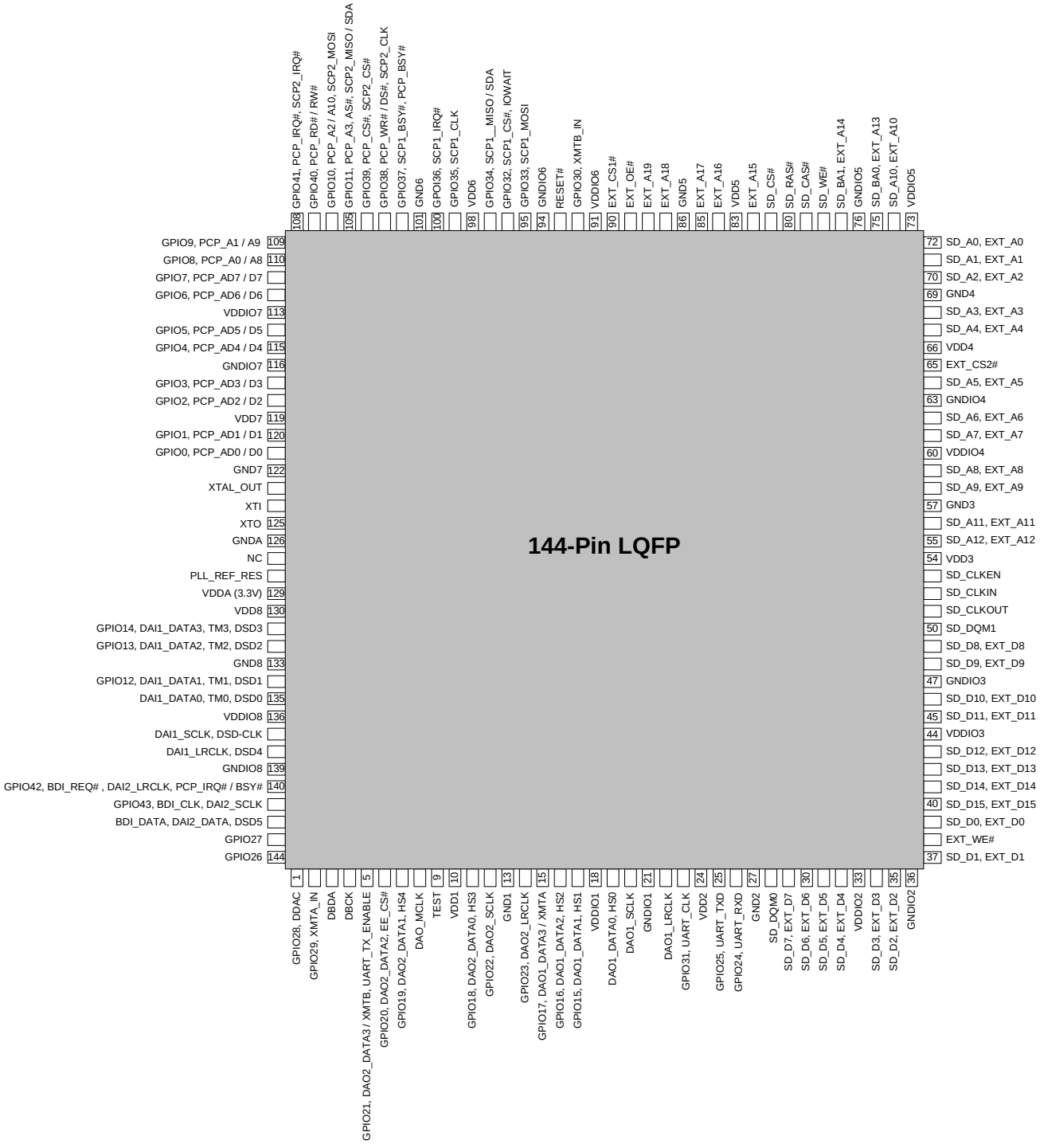


Figure 22. 144-Pin LQFP Pin-Out Drawing

9. Package Mechanical Drawings

9.1 128-pin LQFP Package Drawing

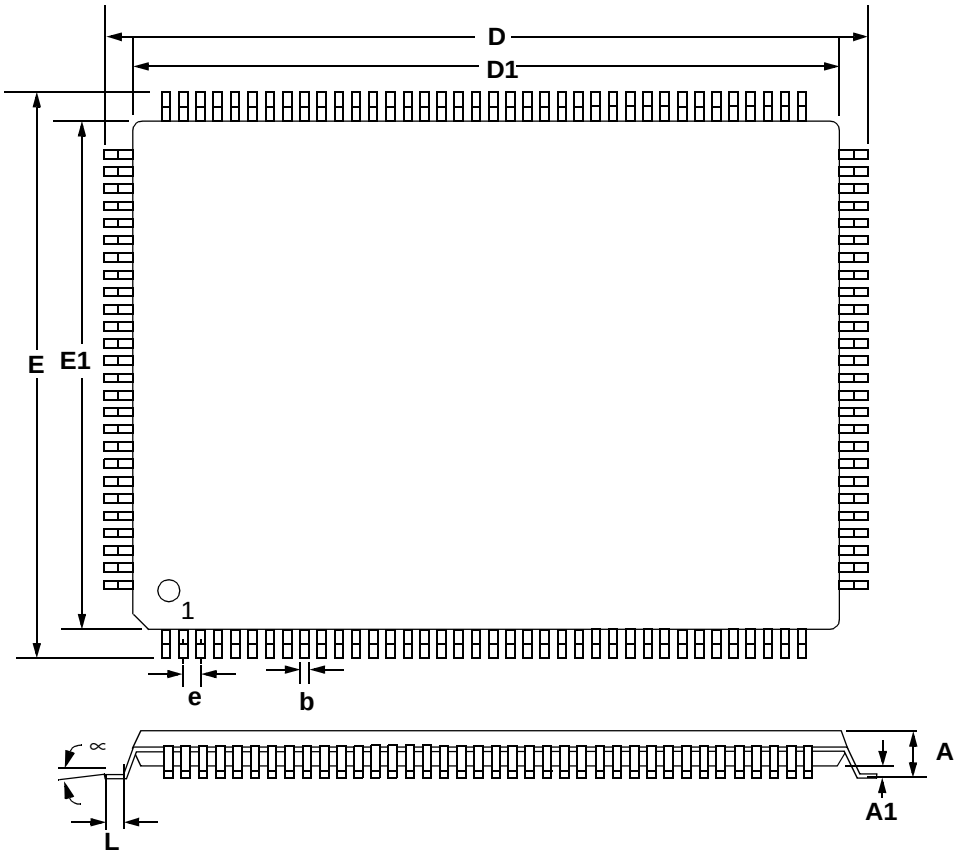
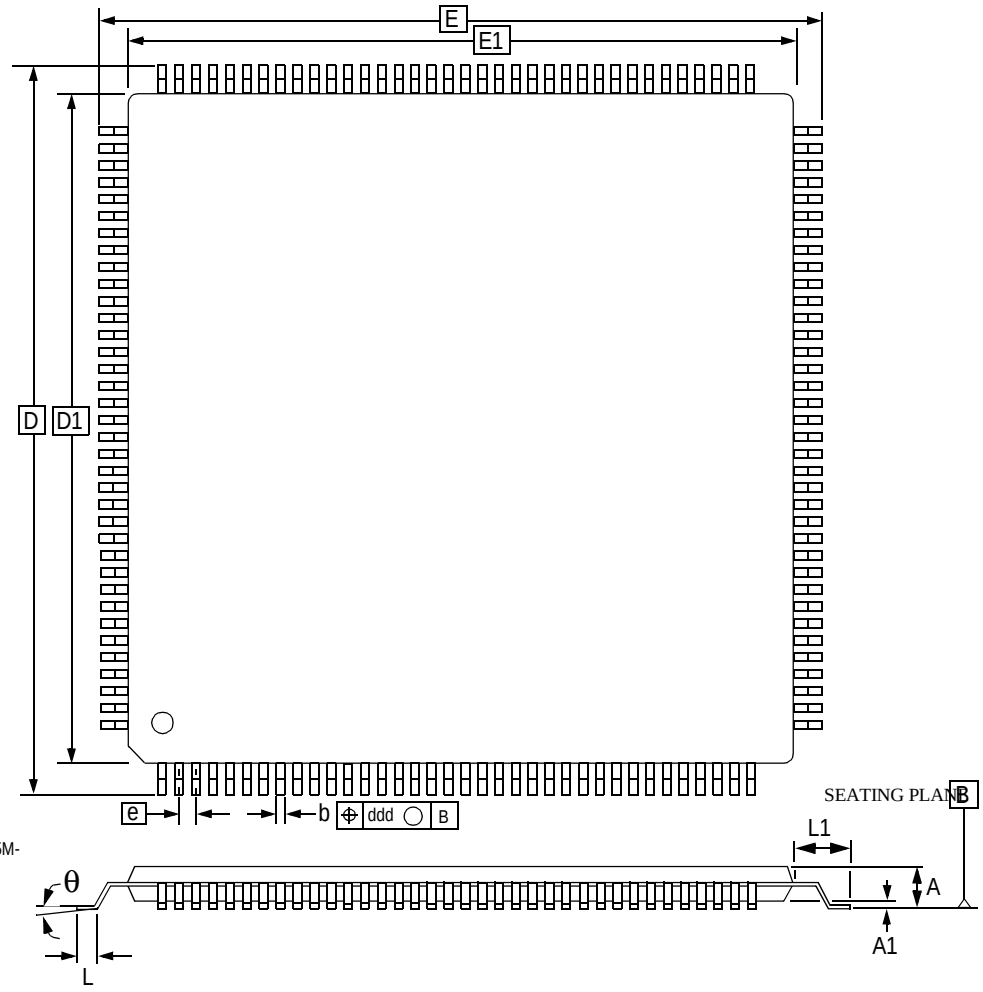


Figure 23. 128-Pin LQFP Package Drawing

Table 7. 128-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	.063”
A1	0.05	---	0.15	.002”	---	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	16.00 BSC			.630”		
E1	14.00 BSC			.551”		
e	0.50 BSC			.020”		
q	0°	3.5	7°	0°	3.5	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

9.2 144-Pin LQFP Package



Notes:

1. Controlling dimension is millimeter.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.

Figure 24. 144-Pin LQFP Package Drawing

Table 8. 144-Pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	.063”
A1	0.05	---	0.15	.002”	---	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	22.00 BSC			.866”		
E1	20.00 BSC			.787”		
e	0.50 BSC			.020”		
q	0°	---	7°	0°	---	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

10. Revision History

Revision	Date	Changes
A1	FEB 2006	Advance release.
A2	JUN 2006	Updated part numbers for ordering (Tables 5 & 6), Updated V_{OH} and V_{OL} specification to include the current load used for testing
A3	JUL 2006	Updated part numbers for ordering (Tables 5 &6). Updated text in sections 3 and 4. Updated parameter descriptions in sections 5.1 and 5.3. Updated Tspickl, Tspickh, and Tspidov timing. Corrected Figure SPI Master Timing to use EE_CS#. Added footnote to XTI table. Removed SCLK/LRCLK relative timing from DAI port timing. Removed SCLK/LRCLK slave relative timing from DAO port timing.
A4	OCT 2007	Updated the Tspidsu, Tspickl, and Tspickh timing parameters for master mode SPI. This applies to both SPI ports.
PP1	May 28, 2008	Updated product feature list in Table 2. Updated Figure 21 and Figure 22.
PP2	June 20, 2008	Added typical crystal frequency values in Table Footnote 1 and Max and Min values of F_{xtal}in Section 5.8. Removed DSD Phase Modulation Mode from Section 5.18. Removed reference to MCLK in Section 5.18. Redefined Master mode clock speed for SCP_CLK in Section 5.11.. Redefined DC leakage characterization data in Section 5.3, correcting units of measurement. Modified Footnote 1 under Section 5.10.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com.

